Heterogeneously Integrated Vapor–Liquid–Solid Grown Silicon Probes/(111) and Silicon MOSFETs/(100)

Akihiro Okugawa, Kotaro Mayumi, Akihito Ikedo, Makoto Ishida, and Takeshi Kawano

***Abstract*—In this letter, we report the heterogeneous integration of vertically aligned silicon (Si) microprobe arrays/(111) with MOSFET circuits/(100) by IC processes and subsequent selective vapor–liquid–solid (VLS) growth of Si. A hybrid Si-on-insulator (SOI) substrate with different species of Si layers, e.g., a (100)-top-Si/buried oxide/(111)-handle-Si system, was utilized for the heterogeneous integration technique. MOSFETs were fabricated on (100) top Si, and vertical VLS probes were synthesized at the selectively exposed (111) handle Si. The different Si layers of the MOSFETs and probes were electrically connected by a 3-D metallization technique. In addition, the electrical properties of 3-D metallization and the MOSFETs were investigated. The results indicate potential for heterogeneous integration of VLS probes/(111) and MOSFETs/(100), promising further integrations of numerous microdevices/different species of substrates and CMOS/(100), including fully depleted SOI-CMOS for high-performance electronics, on the same chip.**

***Index Terms*—Heterogeneous integration, MOSFETs, silicon-on-insulator (SOI) substrate, vapor–liquid–solid (VLS) growth.**

I. Introduction

ALL integrated circuit (IC) Industries/Foundry services fabricate silicon (Si) CMOS with a (100) surface orientation due to the advantageous properties of the MOS system such as the highest electron mobility, lower values of interface trapped charges, and fixed oxide charges compared to other surface-orientated Si substrates [e.g., (110) and (111)] [1]–[3]. However, recent advances in micro/nanoelectromechanical systems and other micro/nano sensor/actuator devices have utilized numerous types of Si substrates. (111)-Si and (110)-Si substrates with different mechanical characteristics have been utilized for physical sensor/actuator devices [4], and orientation-dependent Si chemical etchings have realized numerous Si bulk micromachining [5]. In Si-CMOS devices, a hybrid-orientation technology has utilized an integration of NMOSFETs/(100) and PMOSFETs/(110) on the same substrate using a hybrid-orientation substrate bonded wafer (110/100 or 100/110) followed by selective Si epitaxy [2].

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To utilize (111) Si as a device substrate, we have proposed vertically aligned microprobe electrode arrays fabricated by vapor–liquid–solid (VLS) growth of Si. This probe array can be used to penetrate neuronal tissue and to conduct multisite electrical measurements of extracellular signals ($< 100\ \mu$V, < 1 kHz) [6]. However, for advanced neuroscience applications, such as implantable medical devices, the on-chip microelectronics, including a preamplifier array and site-selector circuitry, must be further integrated before realizing a single-chip neural recording system. Although the fabrication of vertically aligned VLS probes requires a (111)-Si-surface-oriented substrate [7], we have developed on-chip microelectronics using MOSFETs/(111)-Si technology [8]. However, the MOSFETs on (111) Si exhibit inferior characteristics to those on (100) Si due to the aforementioned issues [3], [9], [10]. To resolve device characteristics, herein, we propose the utilization of a hybrid silicon-on-insulator (SOI) substrate consisting of a (100)-top-Si/buried oxide (BOX)/(111)-handle-Si wafer system and a 3-D metallization technique without selective Si epitaxy for heterogeneous on-chip integration of VLS Si probe arrays/(111) and MOSFETs/(100).

II. Fabrication

A hybrid 4-in SOI substrate consisting of 5-μm-thick (100)-top-Si (p-type with a resistivity of 1–20 $\Omega \cdot$ cm)/2-μm-thick BOX/500-μm-thick (111)-handle-Si wafer (p-type with a resistivity of 1–20 $\Omega \cdot$ cm) system was used to fabricate the device. First, the (100) top Si was selectively etched by a tetramethylammonium hydroxide (TMAH) solution to form a gradual Si slope with an angle of 54.7°, which allowed subsequent 3-D metallization [Fig. 1(a)]. Then, NMOSFETs were fabricated onto the (100) top Si, and 3-D metal interconnections were formed by sputtering. Finally, Si microprobe arrays were synthesized at the exposed (111)-handle-Si region by VLS growth [Fig. 1(b)]. The on-chip MOSFETs/(100) top Si were fabricated based on in-house 10-μm-gate-length NMOSFET technology with 50-nm-thick SiO_2 gate dielectrics (dry oxidation at 1000 °C for 60 min) and 400-nm-thick heavily doped n-type poly-Si gate electrodes (low-pressure chemical vapor deposition at 625 °C for 60 min), as previously reported [8]. The multiple layered metal system of WSi/TiN/Ti (thicknesses = 300/50/50 nm) deposited by sputtering and patterned by a photolithography technique with contact printing was used as the 3-D metal interconnection for subsequent VLS growth

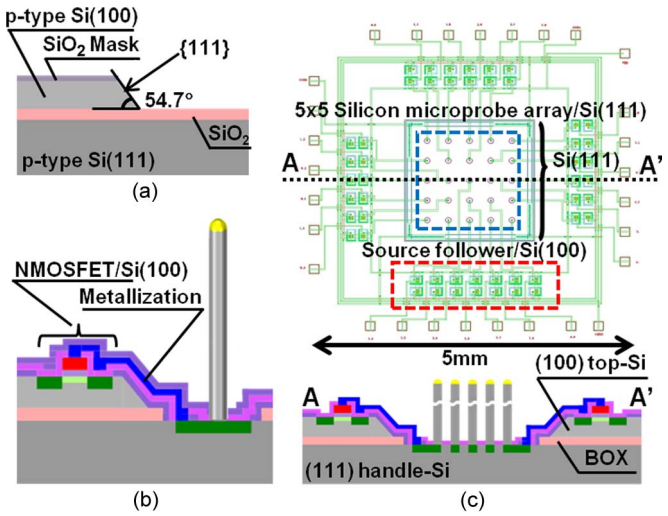

Fig. 1. Process flow for the integration of a VLS probe and a MOSFET using (100)-top-Si/BOX/(111)-handle-Si SOI substrate. (a) Substrate preparation and formation of the top-Si slope by TMAH. (b) NMOSFET process/(100) top Si, 3-D metallization, and Si probe growth/(111) handle Si. (c) Cross-sectional device image through AA′ in CAD layout image. A 5 × 5 mm chip consists of a D-NMOS-based source follower array/(100) top Si (surrounding) and a Si probe array/(111) handle Si (center portion, 2 × 2 mm).

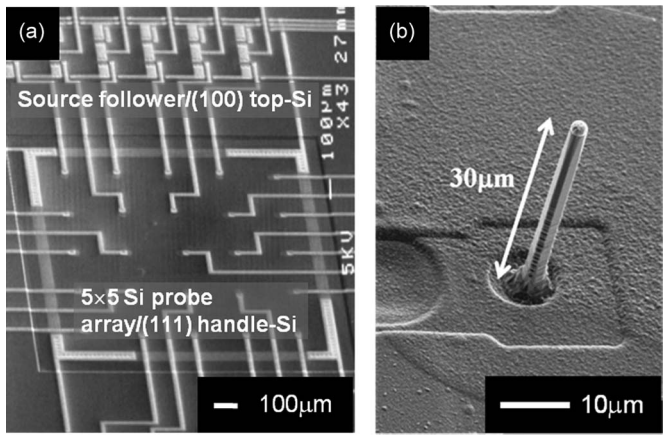

Fig. 2. Integrated VLS-probe array/(111) with MOSFET/(100). (a) SEM image of the fabricated device shown in the CAD in [Fig. 1(c)]. (b) Integrated 3-μm-diameter 30-μm-length Si probe.

(500 °C–700 °C). Herein, the WSi/TiN/Ti system was selected because Ti provides an adhesion layer for SiO_2 and TiN acts as a barrier layer between the Ti and top WSi layers [11]. For neural recordings, headstage voltage buffering amplifiers are commonly used to detect ∼100-μV-amplitude extracellular signals without signal attenuations. In addition, we designed the on-chip headstage amplifier arrays based on the source follower configuration using two depletion-type NMOSFETs (D-NMOS) as the input and the load. Herein, the amplifier arrays are located at the (100)-top-Si region, which surrounds the center region of a 5 × 5 VLS-probe array (2 × 2 mm), as shown in the layout image [Fig. 1(c)]. The threshold voltage of D-NMOS was controlled by ion implantation into the channel region with PF_3 (3×10^{12} cm^{-2}, 60 keV).

Vertical Si microprobe arrays were synthesized at the exposed (111) handle Si in a vacuum chamber system using disilane (Si_2H_6)–phosphine (PH_3) gas as the growth sources and gold (Au) as the growth catalyst. N-type VLS Si probes (impurity concentration of 10^{18} cm^{-3}) have obtained high yields using a mixture gas of 1% PH_3 (diluted in 99% hydrogen) with 100% Si_2H_6 at a gas pressure of 0.6 Pa and a growth temperature of 700 °C with a growth rate of 1 μm/min [12]. Here, VLS growth was performed using the same growth parameters of 30 min at 700 °C. This temperature is lower than the temperature of the MOSFET process (e.g., ∼1000 °C annealing after ion implantations) to avoid subsequent changes in the junction formations of MOSFETs. Fig. 2(a) shows the SEM image of the device overview after the MOSFET fabrication, whereas Fig. 2(b) shows the SEM image of an integrated single VLS probe at the exposed part of (111) handle Si. The probe diameter and length were set to 3 and 30 μm, respectively, for use in low invasive probe penetration into thin tissues such as retinas, peripheral nerves, sliced brain samples, etc. [6], [11]. Using a Au probe-tip coating, we have realized an electrical probe impedance of less than 10 MΩ in saline (1 kHz) [11], which is in the impedance range for neural signal recording [6].

III. Three-Dimensional Interconnection

MOSFETs and probes were fabricated at different Si layers; the height difference between the top-Si and handle-Si wafers was 7 μm (5-μm-thick top Si + 2-μm-thick BOX). Therefore, the metallization technique for the different Si layers [13] is necessary to electrically connect the MOSFETs and VLS probes. To realize the interconnection, we proposed (100)-top-Si etching using TMAH solution, resulting in a gradual Si slope (54.7°) [Fig. 1(a)] [5].

Fig. 3(a) shows the cross-sectional SEM image of a fabricated 360-nm-thick 3-D WSi/TiN/Ti interconnection system over a top-Si slope observed by utilizing focused ion beam sample preparation, demonstrating the uniform thickness of the interconnection. Fig. 3(b) shows the current–voltage characteristics of the formed interconnection (in layout design, width $W = 15$ μm and length $L = 1$ mm, including the two slope shapes [see inset of Fig. 3(b)], indicating a linear behavior with a resistance of 250 Ω. Using the measured WSi/TiN/Ti sheet resistance R_S of 3.43 Ω · cm, the calculated resistance of the formed interconnection is given by $R_S \cdot L/W = 230\ \Omega$, which value is similar to the measured resistance and consistent with the formation result of the conformal 3-D WSi/TiN/Ti metallization over the slopes.

IV. On-Chip MOSFET/(100)

Fig. 3(c) shows the drain current I_{DS}–gate voltage V_{GS} curves of a fabricated NMOSFET/(100) prior to VLS Si probe growth ["Before VLS" in Fig. 3(c)]. After the VLS process [Fig. 1(b)], to terminate the dangling bonds and to decrease the interface states of the MOS system due to plasma processes and thermal annealing in an vacuum environment ["After VLS" in Fig. 3(c)], hydrogen (H_2) annealing at ambient conditions containing 4% H_2 in nitrogen was carried out at 400 °C[8], [14]. Fig. 3(c) also shows the I_{DS}–V_{GS} curves for MOSFETs annealed in H_2 for 30 and 180 min. H_2 annealing caused a

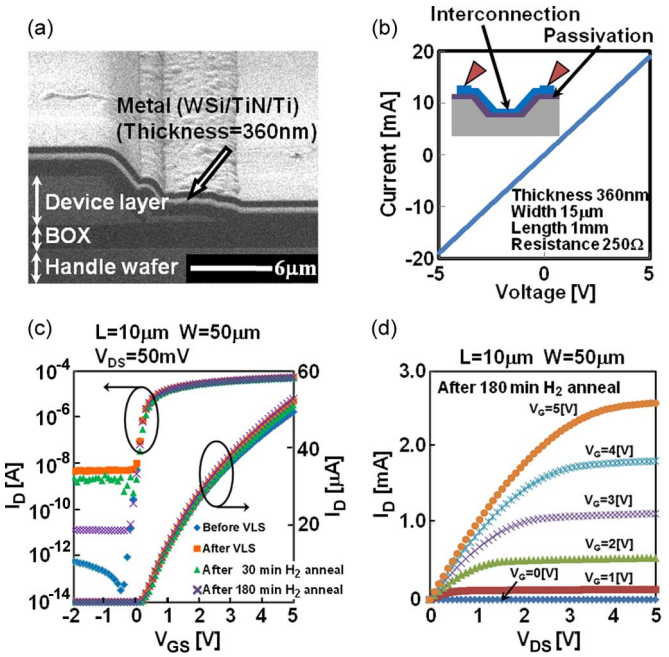

Fig. 3. (a) Cross-sectional SEM image of a 3-D interconnection between the MOSFET/(100) top Si and the VLS Si probe/(111) handle Si. (b) Current–voltage characteristics of a test slope interconnection. (c) Drain current $I_{\rm DS}$–gate voltage $V_{\rm GS}$ characteristics (drain voltage = 50 mV) of fabricated on-chip NMOSFETs/(100) top Si: Before the VLS process and after the VLS process with hydrogen annealing for 0, 30, and 180 min. (d) Drain current $I_{\rm DS}$–drain voltage $V_{\rm DS}$ characteristic of the 180-min hydrogen annealed MOSFET/(100).

nonshifted threshold voltage of 0.2 V with a subthreshold swing of 80 mV/decade (drain voltage = 50 mV). One possibility to reduce the leakage current to less than $\sim 10^{-11}$ A between the drain and the source is to increase the duration of H_2 annealing so that it is longer than 180 min [10]. Fig. 3(d) shows the drain current $I_{\rm DS}$–drain voltage $V_{\rm DS}$ curves of the same 180 min annealed NMOSFET. In addition, the fabricated D-MOS/(100) for the source follower circuit arrays exhibited a controlled threshold voltage of -3.5 V. We measured the D-MOS-based source follower circuit/(100), and a theoretical voltage gain of 0.8 was observed. These characteristics indicate that the proposed heterogeneous integration technique is compatible with MOSFETs/(100).

V. Conclusion

Heterogeneous integration of VLS Si probe arrays/(111) with MOSFETs/(100) has been developed using a hybrid SOI substrate with a (100)-top-Si/BOX/(111)-handle-Si system. The electrical characterizations of on-chip NMOSFETs confirmed the IC compatibility of the proposed process. Another advantage of this integration technique is that non-IC-compatible impurity diffusion on the handle Si, such as the Au catalysis/handle Si for VLS growth in this letter, does not affect the MOSFET characteristics of top Si. Based on the proposed heterogeneous integration technique, fully integrated numerous different substrate-based devices with MOSFETs/(100) Si may realize a new class of microelectronic chips.

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